A Practical AC Large-Signal Model for GaAs Microwave MESFETS

by

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Abstract

An AC large-signal model for the GaAs FET is presented. It incorporates the device geometry and semiconductor properties and relates the terminal currents to the instantaneous applied voltages and their derivatives. Its form is suitable for large-signal component design and optimization.

Introduction

This paper presents a novel AC large-signal model for the GaAs microwave MESFET, whose cross-section is given in Fig. 1. The model is a "true" AC one in the sense that the drain and source total currents are given as explicit functions of the gate-to-source voltage, V_{SG}, the drain-to-source voltage, V_{DS}, and their derivatives:

$$I_D = F_1(V_{DS}, V_{SG}, \frac{dV_{DS}}{dt}, \frac{dV_{SG}}{dt})$$

$$I_G = F_2(V_{DS}, V_{SG}, \frac{dV_{DS}}{dt}, \frac{dV_{SG}}{dt})$$

To our knowledge, this is the first model of its kind. Previous models and simulations were either restricted to DC analysis alone, or to DC analysis with a small signal incremental AC model derived from it (see, for example, [1] - [7]). Some authors have attempted to achieve a "true" AC large signal simulation, but the results have not proven compatible with the need for an efficient model suitable for use with circuit design optimization programs.

The present model is circuit design oriented and can be used to analyze and design large-signal components such as oscillators, power amplifiers, frequency multipliers, mixers, etc. As such it is very efficient and fast on a digital computer. To achieve this, an approximate analytical solution to the device differential equations was developed. Since the model is derived from first principles, it is directly dependent on device geometry and the semiconductor properties.

Description of Model

The analysis is based on the general approach suggested by Yamaguchi and Kodera[8]. The device is subdivided into 3 regions: channel, transition and depletion, and an analytic form for the transition region charge-carrier distribution n(x,y) is assumed. See Fig. 2. This n(x,y) is substituted in Poisson's equation $\nabla^2\Psi = -\frac{q}{\epsilon}(N_D - n)$ and solved for the potential $\Psi(x,y)$. The analytic solution thus achieved is parametric with parameter V_1.

This approach has been used by Yamaguchi and Kodera for DC simulation. We have extended and improved this basic approach in two ways: a) by including the dependence of the currents on the time derivatives of the voltages we have obtained an AC large signal model and b) by solving for the parameter V_1 analytically we have obtained a model which is fast and efficient. Yamaguchi and Kodera solve for V_1 numerically in an iterative fashion. In our model, V_1 is solved analytically. This dramatically shortens the computation time, which is 0.05 seconds per point in our model compared to 1 second for the numerical method.

The output of the model gives the instantaneous drain and source currents for each instantaneous voltage pair (V_{SG}, V_{DS}) in the form

$$I_D = I_{con} + DVSG\frac{dV_{SG}}{dt} + DVDS\frac{dV_{DS}}{dt}$$

$$I_G = GVSG\frac{dV_{SG}}{dt} + GVDS\frac{dV_{DS}}{dt}$$

and includes:

1) the coefficients I_{con}, DVSG, etc., which are functions of V_{DS}, V_{SG}.
2) g_m, the small signal transconductance.
3) g_d, the small signal drain conductance.
4) τ, the transit time.
5) R_C, the gate-source charging resistor.
6) Input and output capacitances.

The circuit diagram of the assembled FET chip is presented in Fig. 3. The "basic" FET chip is the device as characterized by the model above. The other elements are parasitic, part of which are external (L_g, L_d, L_s - wire bond inductances, C_{sin}, C_{so} - parasitic capacitances, R_g - gate metalization resistance) and part of which are internal and calculated by the model (R_{ss}, R_{sd} - bulk resistances on the source and drain sides, R_c - gate source charging resistor). The model includes an ideal diode to permit gate conduction, which occurs in practice for the heavily driven amplifier or in other large signal components.

Only modest memory is required (~ 50K on IBM 360). The current limitations of the model are:

1) Only uniform doping of the channel
2) Substrate effects handled externally (resistor).
3) No negative conductivity assumed in the gate region.
4) No high electric field region between gate and drain contacts.

Large-Signal Results

Using the model, voltage and current waveforms were generated for a FET loaded with 50Ω and driven by an ideal voltage generator with 50Ω source impedance for several values of the generator voltage. See Fig. 4. The device and circuit parameters are given in Tables 1 and 2. The waveforms were Fourier analyzed and the output harmonic power versus incident power was calculated and is shown in Fig. 5.

The use of this model permits one to study the interaction between the device with its parasitics and its external circuit. For example, we are now investigating oscillator build-up waveforms, and frequency multipliers. The effects of the device design on circuit performance can also be established. Because of its speed and efficiency this modeling may find significant application in the development of large-signal microwave FET components.

Acknowledgement: This work was supported in part by the Office of Naval Research under contract N00014-78-C-0265. The authors wish to thank Mr. Harry Willing of the Naval Research Laboratories for his continued interest in this work, and for numerous helpful discussions.

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Table I - Device Parameters

Gate-Source Separation	l_{gs} = 1.7μm
Gate Length	l_g = 1.7μm
Gate-Drain Separation	l_{gd} = 1.7μm
Gate Width	W = 600μm
Doping Level	N_D = 7.5 x10^{16} cm^{-3}
Critical Field	E_C = 3.2 KV/cm
Saturated Velocity	V_S =1.36 x 10^7cm/sec
Relative Dielective Constant	ϵ_r = 12.5
Built-in Potential	ϕ_B = 0.7 V
Gate Metallization Resistance	R_g = 2Ω
Substrate Leakage Resistance	R_{SUB} = 2 x 10^5 Ω
Epitaxial Layer Thickness	a = 0.26 μm

Table 2 - Package/Circuit Parameters

Characteristic Impedance	Z_o = 50Ω
Source Inductance	L_S = 0.1 nH
Gate Inductance	Lg = 0.5 nH
Drain Inductance	L_d = 0.27 nH
Parasitic Input Capacitance	C_{sin} = 0.15 pF
Parasitic Output Capacitance	C_{so} = 0.15 pF

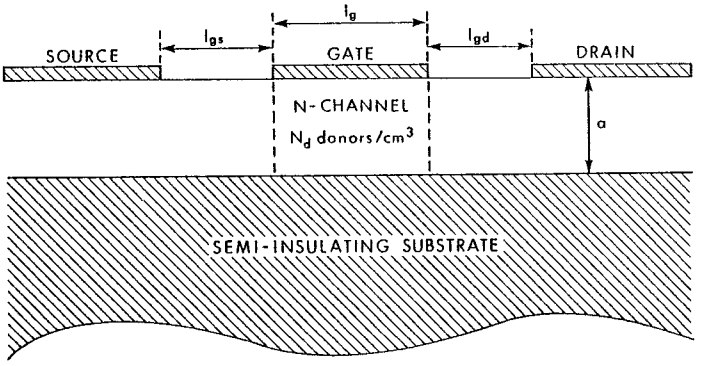


Fig. 1. Cross-section of a typical microwave MESFET.

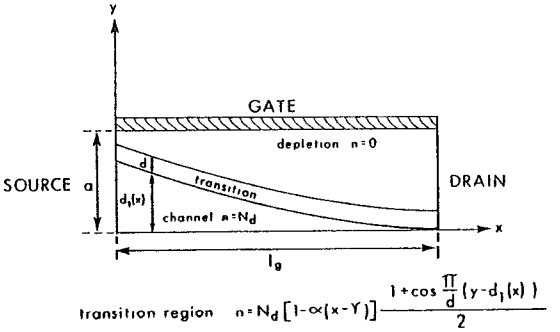
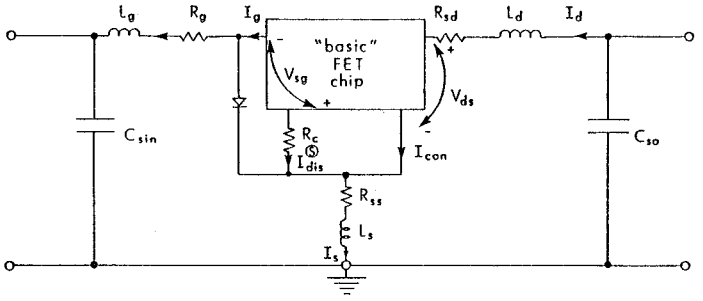


Fig. 2. MESFET division into 3 regions.

Fig. 3. ASSEMBLED FET CHIP MODEL



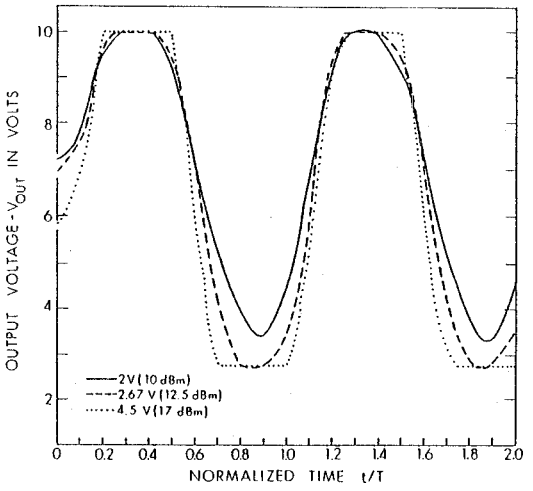


Fig. 4. Output voltage waveform of a typical microwave MESFET.

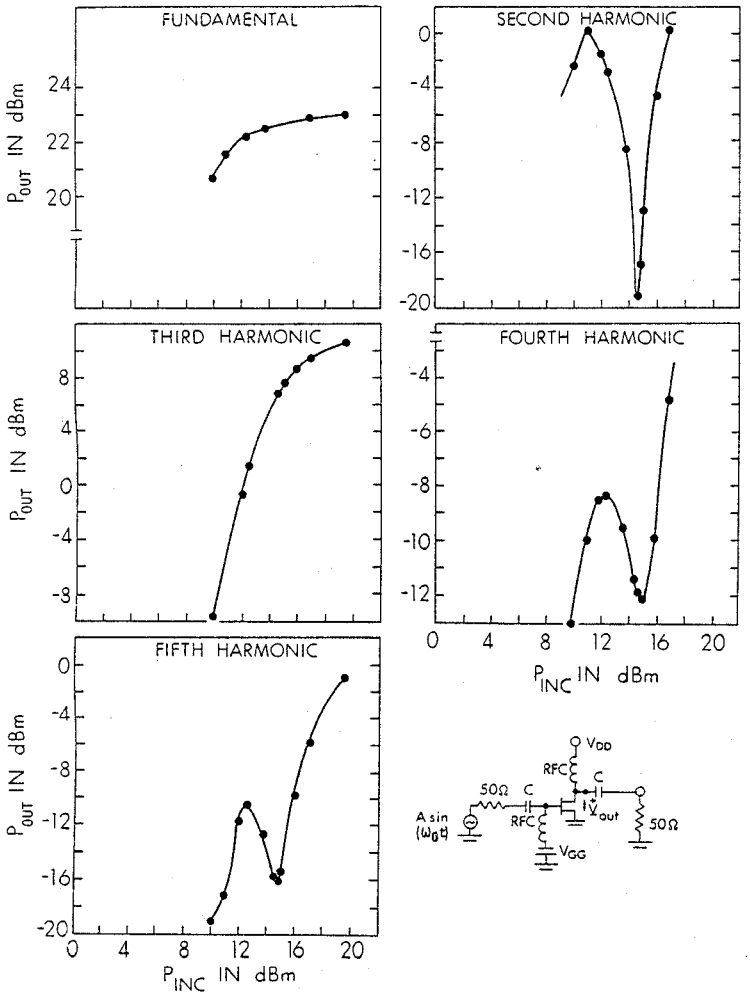


Fig. 5. Fourier analysis of the output voltage waveform.